

Abstract

Memory module having a plurality of integrated memory components

5 A memory module (1) comprises a plurality of integrated memory components (10 to 18, 20 to 28) which are arranged on a carrier substrate. An access control circuit (30), which is arranged separately from the memory components on the carrier substrate, is connected, on the input side, to terminals (40) for supplying address and command signals and, on the output side, to the plurality of integrated memory components (10 to 10 18, 20 to 28). The access control circuit (30) is designed in such a manner that, when supplying an address signal (ADR), it receives an address for a memory access to a selected memory component, respectively generates, from the address received, at least one column address (CADR) and row address (RADR) for the purpose of accessing a bit line (BL) and word line (WL) of the selected memory component and transmits said 15 addresses to the latter. This makes it possible to reduce the design complexity of a memory controller to be provided in a data processing system.

Figure 1